## LISTING OF CLAIMS

This is the current listing of claims in the application.

1-15. (Cancelled)

16. (Previously Presented) An apparatus, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to the at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks;

wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively;

wherein the number of cycles is six, and wherein:

the first cycle indicates first, third, fifth, and seventh memory banks are selected, with an offset of zero;

the second cycle indicates first, second, fifth, and sixth memory banks are selected, with respective offsets of one, zero, one, and zero;

the third cycle indicates second, third, seventh, and eighth memory banks are selected, with respective offsets of one, zero, one, and zero;

the fourth cycle indicates second, fourth, sixth, and eighth memory banks are selected, with an offset of one;

the fifth cycle indicates first, second, fifth, and sixth memory banks are selected, with an offset of two; and

the sixth cycle indicates second, third, seventh, and eighth memory banks are selected, with an offset of two.

17. (Previously Presented) An apparatus, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to the at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks;

wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively;

wherein the number of cycles is six, and wherein:

the first cycle indicates first, third, and fifth memory banks are selected, with an offset of zero;

the second cycle indicates second, third, and sixth memory banks are selected, with respective offsets of zero, one, and zero;

the third cycle indicates first, fourth, and fifth memory banks are selected, with respective offsets of one, zero, and one;

the fourth cycle indicates second, fourth, and sixth eighth memory banks are selected, with an offset of one;

the fifth cycle indicates first, fourth, and fifth memory banks are selected, with an offset of two; and

the sixth cycle indicates second, third, and sixth memory banks are selected, with an offset of two.

18. (Previously Presented) An apparatus, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to the at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks;

wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively;

wherein the number of cycles is six, and wherein:

the first cycle indicates first and third memory banks are selected, with an offset of zero;

the second cycle indicates second and first memory banks are selected, with respective offsets of zero and one;

the third cycle indicates fourth and third memory banks are selected, with respective offsets of zero and one;

the fourth cycle indicates second and fourth memory banks are selected, with an offset of one;

the fifth cycle indicates first and second memory banks are selected, with an offset of two;

and the sixth cycle indicates third and fourth memory banks are selected, with an offset of two.

19. (Previously Presented) An apparatus, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to the at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks;

wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively;

wherein the number of cycles is ten, and wherein:

the first cycle indicates first and third memory banks are selected, with an offset of zero;

the second cycle indicates second and first memory banks are selected, with respective offsets of zero and one;

the third cycle indicates fourth and third memory banks are selected, with respective offsets of zero and one;

the fourth cycle indicates second and first memory banks are selected, with respective offsets of one and two;

the fifth cycle indicates fourth and third memory banks are selected, with respective offsets of one and two;

the sixth cycle indicates second and fourth memory banks are selected, with an offset of two;

the seventh cycle indicates first and third memory banks are selected, with an offset of three;

the eighth cycle indicates second and first memory banks are selected, with respective offsets of three and four;

the ninth cycle indicates fourth and third memory banks are selected, with respective offsets of three and four; and

the tenth cycle indicates second and fourth memory banks are selected, with an offset of four.

20. (Cancelled)

21. (Previously Presented) An apparatus, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to the at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks; and

a plurality of muxes for receiving the plurality of third values and delivering selected third values to each of the respective plurality of memory banks, the third values selected by the controller.

22. (Previously Presented) An apparatus, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to the at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values; and

a controller directing each of the plurality of third values to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern

determined to allow for deinterleaving by retrieving values from the plurality of memory banks; and

a plurality of tri-state buses connected to the plurality of memory banks, each tri-state bus for receiving a third value, selectable by the controller, and each memory bank operable to store the value of the respective tri-state bus as directed by the controller.

23-28. (Cancelled)

29. (Previously Presented) A wireless communication system including a deinterleaver, comprising:

a mapper receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value, and generating a plurality of third values in response to at least one pair of received symbol values;

a plurality of memory banks, each memory bank adaptable to store one of the third values;

a controller directing each of the plurality of third value to a selected one of the plurality of memory banks for simultaneous storing according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks; and

a plurality of muxes for receiving the plurality of third values and delivering selected third values to each of the respective plurality of memory banks, the third values selected by the controller.

30. (Previously Presented) A method of deinterleaving, comprising:

receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value;

mapping at least a first and second value to a plurality of third values, in response to at least one pair of received symbol values;

receiving the plurality of third values and delivering selected third values to each of the respective plurality of memory banks, the third values selected by a controller; and

simultaneously storing the plurality of third values in a plurality of memory banks according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

31. (Original) The method of claim 30, further comprising:

producing a storing address for one or more memory banks according to the storing pattern, each storing address computed using a base address added to an offset indicated by the storing pattern; and

incrementing the base address by a fixed amount subsequent to completion of each successive iteration of the storing pattern.

32. (Original) The method of claim 30, wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively.

33. (Original) The method of claim 30, further comprising: simultaneously retrieving two or more stored third values from two or more memory banks according to a retrieval address; and incrementing the retrieval address sequentially subsequent to a simultaneous retrieval.

34. (Original) The method of claim 33, further comprising delivering the retrieved stored third values to a decoder for subsequent decoding therefrom.

35. (Previously Presented) A device, comprising:

means for receiving at least one pair of reeived symbol values, each pair of received symbol values comprising a first value and a second value,

means for mapping at least a first and second value to a plurality of third values, in response to at least one pair of received symbol values;

means for receiving the plurality of third values and delivering selected third values to each of the respective plurality of memory banks, the third values selected by a controller; and

means for simultaneously storing the plurality of third values in a plurality of memory banks according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

36. (Previously Presented) Computer readable media operable to perform the following steps:

receiving at least one pair of received symbol values, each pair of received symbol values comprising a first value and a second value,

mapping at least a first and second value to a plurality of third values, in response to at least one pair of received symbol values;

receiving the plurality of third values and delivering selected third values to each of the respective plurality of memory banks, the third values selected by a controller; and

simultaneously storing the plurality of third values in a plurality of memory banks according to a storing pattern, the storing pattern determined to allow for deinterleaving by retrieving values from the plurality of memory banks.

37. (Previously Presented) The apparatus of claim 21, wherein the first and second values are in-phase (I) and quadrature (Q) values, respectively.

38. (Previously Presented) The apparatus of claim 21, wherein the third values are soft decision values.

39. (Previously Presented) The apparatus of claim 21, wherein the third values are Log Likelihood Ratio (LLR) values.

40. (Previously Presented) The apparatus of claim 21, the number of memory banks being equal to twice the number of third values.

41. (Previously Presented) The apparatus of claim 21, wherein two or more stored third values may be retrieved from two or more of the plurality of memory banks simultaneously.

42. (Previously Presented) The apparatus of claim 21, wherein the controller directs the plurality of third values for storage in the plurality of memory banks using a storage pattern selectable from a plurality of storage patterns, the storage pattern selected in accordance with one of a plurality of transmission formats.

43. (Previously Presented) The apparatus of claim 42, wherein the plurality of transmission formats comprises 16 Quadrature Amplitude Modulation (QAM).

44. (Previously Presented) The apparatus of claim 42, wherein the plurality of transmission formats comprises rate 1/3 encoding.

45. (Previously Presented) The apparatus of claim 21, wherein the plurality of memory banks are sized in accordance with one or more encoder packet sizes.

46. (Previously Presented) The apparatus of claim 21, wherein the storing pattern comprises a plurality of cycles, each cycle indicating a selected subset of the plurality of memory banks and an address offset value for each memory bank in the selected subset, each of the memory banks in the selected subset for storing one of the plurality of third values, respectively.

47. (Previously Presented) The apparatus of claim 46, wherein the bank selection, offset selection, and third value selection are assigned in accordance with an encoding sequencing pattern.

48. (Previously Presented) The apparatus of claim 46, wherein the number of cycles in a storage pattern is twice the number of encoded symbols in an associated encoding sequence pattern.

49. (Previously Presented) The apparatus of claim 21, wherein the controller produces a storing address for one or more memory banks according to the storing pattern, each storing address computed using a base address added to an offset indicated by the storing pattern, the base

address incremented by a fixed amount subsequent to completion of each successive iteration of the storing pattern.

50. (Previously Presented) The apparatus of claim 49, wherein the base value is set to an initial value and reset to the initial value once a predetermined number of third values have been stored.

51. (Previously Presented) The apparatus of claim 21, wherein the controller selects two or more memory banks for simultaneous retrieval of stored third values according to an address, the address being incremented sequentially subsequent to each simultaneous retrieval.

52. (Previously Presented) The apparatus of claim 21, further comprising a decoder for receiving a series of two or more fourth values and decoding a plurality of fifth values therefrom.

53. (Previously Presented) The apparatus of claim 52, wherein the decoder is a turbo decoder.

54. (Previously Presented) The apparatus of claim 21, further comprising a demodulator for demodulating a received signal to produce the first and second values.

55. (Previously Presented) An apparatus comprising:

a mapper configurable to calculate a plurality $N$ of metric values for each of a plurality of received symbols, each symbol representing $N$ bits of information according to a specified transmission format;

a plurality $N$ of odd memory banks, and a plurality $N$ of even memory banks, each memory bank capable of storing a plurality of metric values, a plurality $N$ of the memory banks capable of being, during the same cycle, separately addressed and separately written to;

a controller configurable to direct each of the plurality $N$ of calculated metric values for each received symbol to be written to $N$ selected ones of the plurality $2N$ of odd and even memory banks, the controller selecting the $N$ memory banks according to a deinterleaving storing pattern.

56. (Previously Presented) The apparatus of claim 55, the controller configurable to direct the *N* selected memory banks to be written to during a single cycle.

57. (Previously Presented) The apparatus of claim 55, each received symbol comprising an in-phase (I) and a quadrature (Q) value.

58. (Previously Presented) The apparatus of claim 55, the transmission format comprising 16 Quadrature Amplitude Modulation (QAM), and *N* being 4.

59. (Previously Presented) The apparatus of claim 55, the transmission format comprising rate 1/3 encoding.

60. (Previously Presented) The apparatus of claim 55, the metric values being soft decision values.

61. (Previously Presented) The apparatus of claim 55, the metric values being Log Likelihood Ratios (LLR's).

62. (Previously Presented) The apparatus of claim 55, the mapper further configurable to calculate a plurality *M* of metric values for each of a second plurality of received symbols, each of the second plurality of symbols representing *M* bits of information according to a second transmission format; and the controller further configurable to direct each of the plurality *M* of calculated metric values for each of the second plurality of symbols to be written to *M* selected ones of the plurality 2*N* of odd and even memory banks, the plurality *M* being less than the plurality *N*.

63. (Previously Presented) The apparatus of claim 55, the controller further configurable to direct memory access of at least an odd memory bank and a corresponding even memory bank during the same cycle to provide at least two stored metric values to a decoder.

64. (Previously Presented) A wireless communication system including a communication device, the device comprising:

a mapper configurable to calculate a plurality *N* of metric values for each of a plurality of received symbols, each symbol representing *N* bits of information according to a specified transmission format;

a plurality *N* of odd memory banks, and a plurality *N* of even memory banks, each memory bank capable of storing a plurality of metric values, a plurality *N* of the memory banks capable of being, during the same cycle, separately addressed and separately written to;

a controller configurable to direct each of the plurality *N* of calculated metric values for each received symbol to be written to *N* selected ones of the plurality 2*N* of odd and even memory banks, the controller selecting the *N* memory banks according to a deinterleaving storing pattern.

65. (Previously Presented) A method for deinterleaving comprising:

calculating a plurality *N* of metric values for each of a plurality of received symbols, each symbol representing *N* bits of information according to a specified transmission format;

directing each of the plurality *N* of calculated metric values for a single received symbol to be written to *N* selected ones of a plurality *N* of odd memory banks and a plurality *N* of corresponding even memory banks, each memory bank capable of storing a plurality of metric values, a plurality *N* of the memory banks capable of being, during the same cycle, separately addressed and separately written to.

66. (Previously Presented) The method of claim 65, wherein the *N* selected memory banks are written to during a single cycle.

67. (Previously Presented) The method of claim 65, the *N* selected ones of the plurality 2*N* of odd and even memory banks being chosen based on a deinterleaving storing pattern.

68. (Previously Presented) The method of claim 67, further comprising, during the same cycle, retrieving two or more stored metric values according to a retrieval address, and incrementing the retrieval address sequentially subsequent to the retrieval.

69. (Previously Presented) The method of claim 68, further comprising delivering the retrieved stored metric values to a decoder.

70. (Previously Presented) An apparatus comprising:

means for calculating a plurality of metric values for each of a plurality of received symbols;

means for selectively storing metric values;

means for directing each of the plurality of calculated metric values for a single received symbol to be written during the same cycle to selected ones of the odd and even memory banks according to a deinterleaving storing pattern.

71. (Previously Presented) Computer readable media operable to perform the following steps:

calculating a plurality *N* of metric values for each of a plurality of received symbols, each symbol representing *N* bits of information according to a specified transmission format;

directing each of the plurality *N* of calculated metric values for a single received symbol to be written to *N* selected ones of a plurality *N* of odd memory banks and a plurality *N* of corresponding even memory banks, each memory bank capable of storing a plurality of metric values, a plurality *N* of the memory banks capable of being, during the same cycle, separately addressed and separately written to.